EXPEDITED PROCEDURE - EXAMINING GROUP 2822

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leonard Forbes et al.	Examiner: Michael Trinh
Serial No.:	09/256,643	Group Art Unit: 2822
Filed:	February 23, 1999	Docket: 303.324US2
Title:	TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE	

AMENDMENT & RESPONSE UNDER 37 C.F.R. § 1.116

Box RCE
Commissioner for Patents
Washington, D.C. 20231

In response to the final Office Action dated 4 January 2001, please amend the application as follows:

This response is accompanied by a Petition, as well as the appropriate fee, to obtain a one-month extension of the period for responding to the final Office Action, thereby moving the deadline for response from 4 April 2001 to 4 May 2001.

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. Specific amendments to individual claims are detailed in the following marked up set of claims.

Please amend the claims as follows:

43. (Twice Amended) A method of fabricating a transistor comprising:

forming a source region and a drain region in a substrate that are separated by a channel region in the substrate;

forming an insulating layer on [a] the substrate;

forming a layer of a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer wherein x is between 0 and 1.0; and

removing portions of the insulating layer and the layer of the silicon carbide compound $Si_{1-x}C_x$ to form a gate on the substrate.